## WHAT IS CLAIMED IS:

	1	1. An integrated circuit, comprising:
	2	a first transistor;
	3	an analog-to-digital converter coupled to the first transistor;
	4	a digital encoder circuit coupled to receive output signals of the analog-to
	5	digital-converter; and
	6	an impedance matching circuit coupled to receive output signals of the digital
	7	encoder circuit, wherein the impedance matching circuit comprises a plurality of second
`	8	transistors coupled in parallel.
10	1	2. The integrated circuit of claim 1 wherein the first transistor is coupled
B.	<b>\</b> <sub>2</sub>	to a resistor.
	≟ ⊒ 1	The intermedial circuit of claim 1 wherein the immediance motching
		3. The integrated circuit of claim 1 wherein the impedance matching
=	<u></u>	circuit is coupled in parallel with an I/O pin of the integrated circuit.
11077 <sup>43</sup> 41117 <sup>40</sup>	= 1 = 2 = 1	4. The integrated circuit of claim 1 wherein the impedance matching
=	<b>1</b> 2	circuit is coupled in series with an I/O pin of the integrated circuit.
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# # # # # # # # # # # # # # # # # # #	≟,l ≟ a	5. The integrated circuit of claim 4 wherein the impedance matching
1	2 ==	circuit is coupled to a buffer circuit that is coupled to the I/O pin.
	1 <sup>2</sup> 1 11	6. The integrated circuit of claim 1 further comprising a plurality of
	2	impedance matching circuits coupled to receive output signals of the digital encoder circuit,
,	3	wherein the plurality of impedance matching circuits each comprises a plurality of transistors
	4	coupled in parallel.
	1	7. The integrated circuit of claim 1 wherein the analog-to-digital
	2	converter comprises a plurality of comparators that provide the analog-to-digital converter
	3	output signals.

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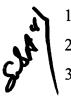
1	9. The integrated circuit of claim 1 wherein the plurality of second
2	transistors of the impedance matching circuit comprises four transistors coupled in parallel.
	10. The integrated circuit of claim 1 wherein the plurality of second
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2	transistors of the impedance matching circuit comprises five transistors coupled in parallel.
1	11. A method for providing impedance matching to a pin of an integrated
2	circuit using an impedance matching circuit, the method comprising:
3	generating a first signal in response to an impedance of a first transistor;
4	converting the first signal into a plurality of second signals; and
5	setting an impedance of the impedance matching circuit in response to the
6	plurality of second signals, wherein the impedance matching circuit is part of the integrated
7	circuit.
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1	12. The method of claim 11 wherein generating the first signal comprises
2	generating the first signal from a resistor divider circuit that comprises the first transistor and
3	a resistor.
1	13. The method of claim 11 wherein converting the first signal in to a
2	plurality of second signals comprises converting the first signal into a plurality of digital
3	signals using an analog-to-digital converter.
1	14. The method of claim 13 wherein converting the first signal in to a
2	plurality of second signals further comprises converting the plurality of digital signals into
3	the plurality of second signals using a digital encoder circuit.
1	15. The method of claim 14 wherein the digital encoder circuit converts
2 ·	the digital signals into the plurality of second signals that are a binary bit representation of the
3	digital signals.
1	16. The method of claim 11 wherein setting the impedance of the
2	impedance matching circuit further comprises causing each one of a plurality of second
3	transistors to be ON or OFF in response to the plurality of second signals.
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The method of claim 16 wherein the plurality of second transistors

comprises at least four transistors coupled in parallel.

		18. The method of claim 11 wherein the impedance matching circuit
	1	
	2	comprises at least five transistors coupled in parallel.
		19. The method of claim 11 wherein setting the impedance of the
	1	impedance matching circuit further comprises setting the impedance of a plurality of
	2	impedance matching circuits wherein each one of the plurality of impedance matching
	3	circuits comprises a plurality of transistors coupled in parallel.
1	4	
\	1	20. The method of claim 19 wherein the plurality of impedance matching
\	2	circuits are coupled in series or in parallel with respect to an associated I/O pin of the
,	3	integrated circuit.
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	1	21. An integrated circuit comprising:
1. ]	2	programmable logic circuitry;
	3	a first transistor for generating an analog signal;
== == ==	4	circuitry for generating a plurality of digital signals in response to the analog
	5	signal, wherein the circuitry includes an analog-to-digital converter, and the digital signals
M	6	comprise a binary representation of the analog signal; and
	7	an impedance matching circuit comprising a plurality of second transistors,
	8	wherein each of the second transistors is coupled to receive one of the digital signals.
		22. The integrated circuit of claim 21 further comprising a plurality of
	1	impedance matching circuits, each comprising a plurality of transistors that are each coupled
-	2	
	. 3	to receive one of the digital signals.
	1	23. The integrated circuit of claim 22 wherein each of the impedance
	2	matching circuits are associated with an I/O pin of the integrated circuit.
	-	1 in the foliage 23 wherein a subset of the impedance
	1	
	2	
	]	25. The integrated circuit of claim 23 wherein a subset of the impedance
		the support of the I/O pins.
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- 27. The integrated circuit of claim 21 wherein the first transistor is coupled to an off-chip resistor, and wherein the first transistor and the off-chip resistor form a resistor divider.
- The integrated circuit of claim 21 wherein the plurality of second transistors comprises at least four transistors coupled in parallel.